IN THE CLAIMS:

1. (Previously Presented) A method of displaying a guard ring within an integrated circuit design having logic devices, said method comprising:

determining positions of said logic devices within said integrated circuit design;

incorporating said guard ring into said integrated circuit design; and

displaying said logic devices and said guard ring symbolically and schematically in a single integrated display,

wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol,

wherein said parameterized symbol comprises parameters, wherein said parameters comprise at least one of a type of said guard ring and an efficiency of said guard ring.

2-4. (Cancelled).

5. (Previously Presented) The method in claim 30, wherein said displaying of said logic devices and said guard ring graphically comprises illustrating relative positions of said logic devices and said guard ring.

6-12. (Cancelled).

13. (Previously Presented) A method of displaying at least one guard ring within a hierarchical integrated circuit design having logic devices, a parameterized cell, and said at least one guard ring, said method comprising:

establishing positions of said logic devices within a portion of said hierarchical integrated circuit design;

incorporating said guard ring into said portion of said hierarchical integrated circuit design; and

displaying said portion of said integrated circuit design as a cell having said guard ring within said hierarchical integrated circuit design,

wherein said displaying of said portion of said integrated circuit design comprises displaying said logic devices and said guard ring symbolically and schematically in a single integrated display,

wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol,

wherein said parameterized symbol comprises parameters, wherein said parameters comprise at least one of a type of said guard ring and an efficiency of said guard ring.

14-16. (Cancelled).

17. (Original) The method in claim 13, wherein said displaying of said portion of said integrated circuit design comprises graphically illustrating relative positions of said logic devices and said guard ring.

18-24. (Cancelled).

25. (Previously Presented) A program storage device readable by machine, tangibly embodying a program of instructions executable by the machine to perform a method of displaying a guard ring within an integrated circuit design having logic devices, said method comprising:

determining positions of said logic devices within said integrated circuit design;

incorporating said guard ring into said integrated circuit design; and

displaying said logic devices and said guard ring symbolically and schematically in a single integrated display,

wherein said displaying of said logic devices and said guard ring symbolically comprises displaying a parameterized symbol,

wherein said parameterized symbol comprises parameters, wherein said parameters comprise at least one of a type of said guard ring and an efficiency of said guard ring.

26-28. (Cancelled).

29. (Previously Presented) The program storage device in claim 39, wherein said displaying of said logic devices and said guard ring graphically comprises illustrating relative positions of said logic devices and said guard ring.

30. (Previously Presented) The method in claim 1, further comprising displaying said logic

devices and said guard ring graphically in said single display.

31-32. (Cancelled).

33. (Previously Presented) The method in claim 1, wherein said displaying of said parameterized symbol comprises displaying said parameters including a type of circuit.

34. (Cancelled).

35. (Previously Presented) The method in claim 1, wherein said displaying of said parameterized symbol comprises displaying said parameters including a type of circuit and an efficiency of said guard ring.

36. (Previously Presented) The method in claim 13, wherein said displaying of said parameterized symbol comprises displaying said parameters including a type of circuit.

37. (Cancelled).

38. (Previously Presented) The method in claim 13, wherein said displaying of said parameterized symbol comprises displaying said parameters including a type of circuit and an efficiency of said guard ring.

39. (Previously Presented) The program storage device in claim 25, further comprising displaying said logic devices and said guard ring graphically in a single display.

40-41. (Cancelled).

42. (Previously Presented) The program storage device in claim 25, wherein said displaying of said parameterized symbol comprises displaying said parameters including a type of circuit.

43. (Cancelled).

44. (Previously Presented) The program storage device in claim 25, wherein said displaying of said parameterized symbol comprises displaying said parameters including a type of circuit and an efficiency of said guard ring.